In The Specification:

Please amend the paragraph beginning at line 13 of page 6 as follows:

If the high level of the reset gate is VDD, the reset transistor [[~~40~~]] 20 turns off slowly as the PD voltage reaches VDD-Vr duering reset. Vt is the reset transistor threshold voltage. The final voltage on PD will depend on the width of the reset pulse 70 as well as the starting voltage of PD 80. This will be referred to as "soft reset". If for example a pixel is bright in one frame but dark in the next, the signal that is measured Vsig-Vrst2 100 will be higher than the actual accumulated signal Vsig-Vrst1 90.